CLAIMS

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A method for determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero.

2. A method according to Claim 1 for adjusting a local clock of a digital data decoder, wherein the clock oscillates at a local clock frequency, the method further comprising the steps of:

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify the program clock value and frequency;

maintaining a program clock value based on the clock signals received at the decoder;

determining if there is any difference between the local clock and the program clock frequencies;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is either a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and

the program clock value, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero.

3. A method according to Claim 2, wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the processor to adjust the local clock frequency.

4. A method according to Claim 3, wherein the threshold condition is a function of the difference between the local clock value and the program clock value.

5. A method according to Claim 3, wherein the step of using the processor to adjust the local clock frequency includes the steps of:

monitoring for the occurrence of the threshold condition; and

transmitting a signal to the processor when the threshold condition occurs.

6. A system for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the system comprising:

means for maintaining a local clock value based on the oscillations of the local clock;

means for receiving clock signals transmitted to the decoder at a program clock frequency;

means for maintaining a program clock value based on the clock signals transmitted to the decoder;

means for determining if there is any difference between the local clock and the program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and the program clock value, so that said difference approaches zero.

7. A system according to Claim 6, wherein the means for adjusting the frequency at which the local clock oscillates includes:

hardware for adjusting the local clock frequency until a threshold condition occurs; and

a processor having a software program for adjusting the local clock frequency after the threshold condition occurs.

8. A system according to Claim 6, wherein the threshold condition is a function of the difference between the local clock value and the program clock value.

9. A system according to Claim 7, wherein the processor is not used to adjust the local clock frequency until the threshold condition occurs.

10. A system according to Claim 7, said hardware includes:

means for monitoring for the occurrence of the threshold condition; and

means for transmitting a signal to the processor when the threshold condition occurs.

11. A method for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the method comprising the steps of:

maintaining a local clock value based on the oscillations of the local clock;

receiving clock signals at the decoder at a program clock frequency;

maintaining a program clock value based on the clock signals received at the decoder;

using the previous clock values to calculate the exact difference in frequency; and

adjusting the frequency at which the local clock oscillates so that said difference approaches zero.

12. A method according to Claim 11, wherein the using step includes the step of using both the difference in the clock frequency and the difference between the local clock value and the program clock value to calculate the exact difference in frequency.